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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/758,040	CHOI, SUNG-KYU	
	Examiner	Art Unit	
	Christopher E. Lee	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 26th of October 2006. Claims 1 and 10 have been amended; no claim has been canceled; and no claim has been newly added since the Non-Final[2] Office Action was mailed on 26th of June 2006. Currently, claims 1-10 are pending in this Application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bourke et al. [US 5,509,124 A; hereinafter Bourke] in view of Barrenscheen et al. [US 2003/0084226 A1; Barrenscheen].

Referring to claim 1, Bourke discloses a buffering apparatus (i.e., IOIC 10j-m in Fig. 2, standing for Input Output Interface Controller) comprising:

- an asynchronous data bus write unit (i.e., means for processing storage read command in storage operation control 40b2 in Fig. 16) which, when control information (i.e., during control signal ACTIVATE READY being **not asserted**) indicating a request for writing in a buffer (i.e., loading data into registers and buffers 20 of Fig. 2) connected to an asynchronous data bus (i.e., SPD bus 10t-w in Fig. 2) not synchronized with a processor (i.e., instruction processor unit 10a of Fig. 1) is provided by a multiplexer (i.e., adapter interface 14 of Fig. 2A with adapter bus control logic 30 of Fig. 2) connected to the

processor (i.e., said instruction processor unit; See col. 17, lines 59-64), receives third data (i.e., data being read from common memory facility 10d in Fig. 1) from the multiplexer (i.e., said adapter interface with adapter bus control logic, in fact said adapter bus delivering said data), stores the third data (i.e., loading said data into said registers and buffers; See col. 17, lines 59-61), and transfers the stored third data to a second memory (i.e., IOBU 10p-s in Fig. 1, standing for Input Output Bus Unit, e.g., serial presence detect (SPD) EEPROM) through the asynchronous data bus (i.e., said SPD bus; See col. 17, lines 61-64); and

- an asynchronous data bus read unit (i.e., means for processing storage write command in storage operation control 40b2 in Fig. 16) which, when control information (i.e., control signal DATA IN END being **asserted**) indicating a request for reading from the buffer (i.e., unloading data from said registers and buffers) is provided by the multiplexer (i.e., said adapter interface with adapter bus control logic; See col. 17, lines 50-59), receives fourth data (i.e., data to be written to said common memory facility) from the second memory (i.e., said IOBU, e.g., SPD EEPROM) through the asynchronous data bus (i.e., said SPD bus; See col. 17, lines 50-54), stores the fourth data (i.e., loading said data to be written to said common memory facility into said registers and buffers; See col. 17, line 55), and transfers the stored fourth data to the multiplexer (i.e., said adapter interface with adapter bus control logic; See col. 17, lines 55-59).

Bourke does not teach that the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor.

Barrenscheen discloses a data transmission device (i.e:, data transmission unit in Fig. 1; See Abstract, paragraph [0001]), wherein

- a multiplexer (i.e., Bus Interface BI1 in Fig. 4) receives first data from a processor (e.g., Module BU11 in Figs. 2A-B; See paragraph [0029]) and transfers the received first data to a first memory (e.g., Module BU12 in Figs. 2A-B; See paragraph [0029]) through a synchronous data bus (i.e., BUS1 in Figs. 2A-B) synchronized with the processor (See paragraph [0035], lines 11-12; for example, DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A), or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor (See paragraph [0035], lines 11-12; for example, DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data transmission device (i.e., data transmission unit), as disclosed by Barrenscheen, in said buffering apparatus (i.e., Input Output Interface Controller), as disclosed by Bourke, for the advantage of providing a way of transmitting large volumes of data quickly and efficiently with a low level of involvement (See Barrenscheen, paragraph [0011]).

4. Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki et al. [JP 2000-92365 A; cited by the Applicant; hereinafter Masayuki] in view of Barrenscheen [US 2003/0084226 A1].

Referring to claim 2, Masayuki discloses a processor bus connection method (i.e., a method for preventing congestion in an image data bus to allow each circuit to efficiently conduct signal processing; See Abstract) comprising:

- (a)' when address information indicating an address of a first memory (i.e., address of recording apparatus 51 of Fig. 2) connected to a synchronous data bus (i.e., CPU bus 34 of Fig. 2) synchronized with a processor (i.e., CPU 41 of Fig. 2), from the processor is received (i.e., addressing command being executed by said CPU), transferring first data (i.e., compressed image data) to the first memory through the synchronous data bus (See paragraph [0029]); and
- (b)' when address information indicating an address of a second memory (i.e., address of image memory 32 of Fig. 2) connected to an asynchronous data bus not synchronized with the processor (i.e., image data bus 33 of Fig. 2), from the processor is received (i.e., addressing command being executed by said CPU), transferring third data (i.e., image data from input device, e.g., CCD image sensor 11 of Fig. 2) to the second memory through the asynchronous data bus (See paragraph [0028]).

Masayuki does not teach (a) when address information indicating the address of the first memory connected to the synchronous data bus, from the processor is received, receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus, or receiving second data from the first memory through the synchronous data bus and transferring the received second data to the processor; and (b) when address information indicating the address of the second memory connected to the asynchronous data bus, from the processor is received, receiving the third data from the processor, transferring the third data, storing the transferred third data, and transferring the stored third data to the second memory through the asynchronous data bus, or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor.

Barrenscheen discloses a method for data transmission forwarding data (See Abstract and paragraph [0001]) comprising:

- (a) when address information indicating an address of a first memory (i.e., address of Module BU12 in Figs. 2A-B) connected to a synchronous data bus (i.e., BUS1 in Figs. 2A-B) synchronized with a processor (i.e., Module BU11 in Figs. 2A-B), from the processor is received (See paragraph [0035], lines 1-4; actually, data transmission between devices connected to said BUS1 in Fig. 2A), receiving first data from the processor and transferring the received first data to the first memory through the synchronous data bus (See paragraph [0035], lines 11-12; for example, DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A), or receiving second data from the first memory through the synchronous data bus and transferring the received second data to the processor (See paragraph [0035], lines 11-12; for example, DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A); and
- (b) when address information indicating an address of a second memory (i.e., address of Module BU23 in Figs. 2A-B) connected to an asynchronous data bus (i.e., BUS2 in Figs. 2A-B) not synchronized with the processor (i.e., said Module BU11, which is synchronized with said BUS1, not said BUS2), from the processor is received, receiving third data from the processor, transferring the third data, storing the transferred third data (i.e., data stored in IM Buffer Store in Fig. 4), and transferring the stored third data to the second memory (i.e., said Module BU23) through the asynchronous data bus (See paragraph [0036]; for example, data writing operation from said Module BU11 to said Module BU23 via bus bridge in Fig. 2B), or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the

stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor (See paragraph [0036]; for example, data reading operation from said Module BU23 to said Module BU11 via bus bridge in Fig. 2B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method for data transmission forwarding data, as disclosed by Barrenscheen, in said processor bus connection method (i.e., a method for preventing congestion in an image data bus to allow each circuit to efficiently conduct signal processing), as disclosed by Masayuki, for the advantage of providing a way of transmitting large volumes of data quickly and efficiently with a low level of involvement (See Barrenscheen, paragraph [0011]).

Referring to claim 3, Barrenscheen teaches (a) comprising

- (a1) when the address information indicating the address of the first memory (i.e., address of Module BU12 in Figs. 2A-B) is provided by the processor (i.e., Module BU11 in Figs. 2A-B) and a control information indicating a request for writing in the first memory is provided by the processor (i.e., DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A), receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus (See paragraph [0035], lines 1-4 and 11-12; i.e., wherein in fact that the data transmission device DTU as a DMA controller in fact transfers data from the device BU11 to the device BU12 clearly anticipates that a control information indicating a request for writing in the first memory is provided by the processor, receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus); and

- (a2) when the address information indicating the address of the first memory (i.e., address of said Module BU12) is provided by the processor (i.e., said Module BU11) and the control information indicating the request for reading from the first memory is provided by the processor (i.e., DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A), receiving the second data from the first memory through the synchronous data bus and transferring the received data to the processor (See paragraph [0035], lines 1-4 and 11-12; i.e., wherein in fact that the data transmission device DTU as a DMA controller can transmit data from one of the devices connected to the bus BUS1 to another of the devices connected to the BUS 1, and said DTU in fact transfers data from the device BU11 to the device BU12, as an example shown in Fig. 2A, clearly anticipates that the control information indicating the request for reading in the first memory is provided by the processor, receiving the second data from the processor and transferring the received data to the processor).

Referring to claim 4, Masayuki discloses a synchronous bus (i.e., CPU bus 34 of Fig. 2) and asynchronous bus (i.e., image data bus 33 of Fig. 2) path method (in fact, a method for preventing congestion in an image data bus to allow each circuit to efficiently conduct signal processing; See Abstract) comprising:

- (a) receiving input data (i.e., receiving image data from CCD image sensor 11 in Fig. 2) and transferring the received input data (i.e., said image data) through an asynchronous data bus (i.e., image data bus 33 of Fig. 2) not synchronized with a processor (i.e., CPU 41 of Fig. 2), then transferring the input data (i.e., compressed image data after said image data being processed by JPEG encoder/decoder 29 in Fig. 2) through a

synchronous data bus (i.e., CPU bus 34 of Fig. 2) synchronized with the processor (i.e., said CPU); and

- (b) receiving the input data (i.e., said compressed image data) through the synchronous bus and transferring the received input data (See paragraph [0029]).

Masayuki does not teach (c) generating first data or third data from the transferred input data and transferring the generated first or third data; (d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing the third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor; (e) receiving the first data through the synchronous bus and storing the data; and (f) receiving the third data through the asynchronous bus and storing the data.

Barrenscheen discloses a synchronous bus and asynchronous bus path method (i.e., a method for data transmission forwarding data on a first and second data busses; See Abstract and paragraph [0001]), wherein a data transmission unit (i.e., DTU in Figs. 2A-B) performs the step of

- (c) generating first data (i.e., data from DTU toward Module BU12 on BUS1 in Fig. 2A) or third data (i.e., data from DTU toward Module BU23 on BUS2 in Fig. 2B) from transferred input data and transferring the generated first or third data (See paragraphs [0034]-[0036]);
- (d) receiving the first data, transferring the received first data to a first memory (i.e., Module BU12 in Figs. 2A-B) through the synchronous data bus (See Fig. 2A and paragraph [0035], lines 11-12), or receiving and storing the third data (i.e., data stored in IM Buffer Store in Fig. 4) and transferring the stored third data to a second memory (i.e., Module BU23 in Figs. 2A-B) through an asynchronous bus (i.e., BUS2 in Figs. 2A-B;

See paragraph [0036]) not synchronized with the processor (i.e., said Module BU11, which is synchronized with said BUS1, not said BUS2);

- (e) receiving the first data through the synchronous bus and storing the first data (See paragraph [0035] and Fig. 2A, wherein data are transferred via DMA controlling, i.e., received and stored through said BUS1 by DMA transferring operation); and
- (f) receiving the third data through the asynchronous bus and storing the third data (See paragraph [0036] and Fig. 2B, wherein data are transferred via bus bridging, i.e., received and stored via said BUS2 by bus bridge transferring operation).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data transmission unit (i.e., DTU), as disclosed by Barrenscheen, in said path between said synchronous bus (i.e., CPU bus) and said asynchronous bus (i.e., image data bus), as disclosed by Masayuki, for the advantage of providing a way of transmitting large volumes of data quickly and efficiently with a low level of involvement (See Barrenscheen, paragraph [0011]).

Referring to claim 5, Masayuki, as modified by Barrenscheen, teaches

- (g) transferring second data through the synchronous bus (i.e., data transferring through BUS1 in Fig. 2A; See Barrenscheen, paragraph [0035], lines 11-12);
- (h) transferring fourth data through the asynchronous bus (i.e., data transferring through BUS2 in Fig. 2B; See Barrenscheen, paragraph [0036]);
- (i) receiving the second data through the synchronous bus and transferring the received second data (See Barrenscheen, paragraph [0035]), or receiving the fourth data through the asynchronous bus, storing the fourth data (i.e., data being stored in IM Buffer Store

in Fig. 4; Barrenscheen), and transferring the stored fourth data (See Barrenscheen, paragraphs [0036] and [0043]);

- (j) generating output data (i.e., OSD image memory 32 generates character image in Fig. 2; Masayuki) from the second data or fourth data (See Masayuki, paragraph [0024]) and transferring the output data (i.e., transferring said generated character image to said memory controller in Fig. 1; Masayuki);
- (k) receiving and storing the output data (i.e., bit map data are stored in said memory controller for controlling) and transferring the stored output data through the asynchronous bus (i.e., transferring said OSD and image data to NTSC/PAL encoder 23 via image data bus 33 for composition in Fig. 2; See Masayuki, paragraph [0024]); and
- (l) receiving the output data through the asynchronous bus (See Masayuki, paragraph [0024]) and outputting the received output data (See Masayuki, paragraphs [0031]-[0033]).

Referring to claim 6, Masayuki teaches

- if the received output data or the received third data is display data (i.e., OSD and/or image data; See paragraph [0024]), the received output data is displayed (i.e., displayed on finder 36 in Fig. 2).

5. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki [JP 2000-92365 A] in view of Barrenscheen [US 2003/0084226 A1] as applied to claims 2-6 above, and further in view of Sodos [US 5,239,651 A].

Referring to claim 7, Masayuki, as modified by Barrenscheen, discloses all the limitations of the claim 7, except that does not expressly teach giving permission on the use of the synchronous bus; and giving permission on the use of the asynchronous bus.

Sodos discloses a method of arbitration for multiple requested data transfers (See Abstract), wherein

- (m) giving permission (i.e., bus grant) on the use of a synchronous bus (e.g., Internal Busses 240 of Fig. 2); and
- (n) giving permission (i.e., bus grant) on the use of an asynchronous bus (e.g., External Busses 230 of Fig. 2; See col. 5, lines 3-33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of arbitration for multiple requested data transfers, as disclosed by Sodos, in said method for said synchronous and asynchronous busses path, as disclosed by Masayuki, as modified by Barrenscheen, for the advantage of providing an efficient resource utilization for a resource handling multiple time multiplexing data transfer operations (See Sodos, col. 2, lines 26-32).

Referring to claim 8, Masayuki, as modified by Barrenscheen and Sodos, teaches

- in (a) and (b), the received input data is transferred through the synchronous bus and the input data is received through the synchronous bus (i.e., data being transferred through BUS1 in Figs. 2A-B; Barrenscheen) for which permission to use is given in (m) (i.e., said BUS1 is granted to transfer said data; See Sodos, col. 5, lines 3-33);
- in (d), the received first data is transferred to the first memory (i.e., data being transferred to Module BU12 in Figs. 2A-B; Barrenscheen) through the synchronous data bus and the first data is received through the synchronous bus and stored (i.e.,

transferred to said Module BU12; See Barrenscheen, Fig. 2A and paragraph [0035], lines 11-12) for which permission to use is given in (m) (i.e., said Module BU12 is granted to transfer said data; See Sodos, col. 5, lines 3-33), or the stored third data (i.e., data stored in IM Buffer Store in Fig. 4; Barrenscheen) is transferred to a second memory (i.e., data being transferred to Module BU23 in Figs. 2A-B; Barrenscheen) through the asynchronous bus (i.e., BUS2 in Figs. 2A-B; See Barrenscheen, paragraph [0036]) for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33);

- in (f), the third data is received through the asynchronous bus (i.e., BUS2 in Figs. 2A-B; See Barrenscheen, paragraph [0036] and Fig. 2B) for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33) and stored (in fact, data are transferred via bus bridging, i.e., received and stored via said BUS2 by bus bridge transferring operation; Barrenscheen).

Referring to claim 9, Masayuki, as modified by Barrenscheen and Sodos, teaches

- in (g), the second data is transferred through the synchronous bus (i.e., data transferring through BUS1 in Fig. 2A; See Barrenscheen, paragraph [0035], lines 11-12) for which permission to use is given in (m) (i.e., said BUS1 is granted to transfer said data; See Sodos, col. 5, lines 3-33);
- in (h), the fourth data is transferred through the asynchronous bus (i.e., data transferring through BUS2 in Fig. 2B; See Barrenscheen, paragraph [0036]) for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33);

- in (i), the second data is received through the synchronous bus (i.e., said BUS1) for which permission to use is given in (m) (i.e., said BUS1 is granted to transfer said data; See Sodos, col. 5, lines 3-33) and the received second data is transferred (See Barrenscheen, paragraph [0035]), or the fourth data is received through the asynchronous bus for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33), stored (i.e., data being stored in IM Buffer Store in Fig. 4; Barrenscheen), and the stored fourth data is transferred (See Barrenscheen, paragraphs [0036] and [0043]);
- in (k) the output data (i.e., bit map data are stored in said memory controller for controlling; Masayuki) is received and stored, and the stored output data is transferred through the asynchronous bus (i.e., transferring said OSD and image data to NTSC/PAL encoder 23 via image data bus 33 for composition in Fig. 2; See Masayuki, paragraph [0024]) for which permission to use is given in (n) (i.e., said image data bus is granted to transfer said data; See Sodos, col. 5, lines 3-33); and
- in (l), the output data is received through the asynchronous bus (See Masayuki, paragraph [0024]) and the received output data is output to a user (i.e., user of digital still camera in Fig. 2; See Masayuki; paragraphs [0031]-[0033]) for which permission to use is given in (n) (i.e., said image data bus is granted to transfer said data; See Sodos, col. 5, lines 3-33) and the received third data is output (i.e., displaying on finder 36 of Fig. 2; Masayuki).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki [JP 2000-92365 A] in view of Barrenscheen [US 2003/0084226 A1] and what was well known in the art, as exemplified by Luo et al. [US 6,265,885 B1; hereinafter Luo].

Referring to claim 10, all of the claim limitations have already been discussed/addressed with respect to claim 4, with the exception of a tangible computer readable recording medium including a computer program having instructions for controlling a synchronous bus and asynchronous bus, the instructions comprising the steps of the method in the claim 4 (e.g., implementing in a computer software program).

The Examiner takes Official Notice that said method in the claim 4 being implemented in a computer program having instructions for controlling said synchronous bus and asynchronous bus (i.e., a computer software program), and being stored in a tangible computer readable recording medium (e.g., ROM; See Application, page 49, line 1), is well known to one of ordinary skill in the art, as evidenced by Luo (See Claim 9, lines 2-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said method of the claim 4 in said computer program having said instructions (i.e., a computer software program), and being stored in said tangible computer readable recording medium (i.e., read-only memory; See Luo, col. 3, lines 38-54) since it would have provided a better flexibility of implementing said method than a hardware implementation, such as an easy modification, etc.

Furthermore, the recitation in the claim 10, that "a tangible computer readable recording medium including a computer program" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *See Kropa v. Robie, 88 USPQ 478 (CCPA 1951).*

Response to Arguments

7. Applicant's arguments filed on 26th of October 2006 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "... The Examiner alleges that Barrenscheen discloses the missing features. Particularly, the Examiner asserts that bus interface BI1 in Fig. 4 is a multiplexer that operates in the manner disclosed in claim 1. However, bus interface BI1 is not a multiplexer. Instead, bus interfaces BI1-BI4 are used to connect the data transmission device DTU to the first through fourth buses BUS1-BUS4, respectively. Consequently, bus interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen." in the Response page 9, lines 6-21, the Examiner respectfully disagrees.

In fact, the Applicant recites the claimed subject matter "multiplexer" with the limitation "wherein the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor" (See Claim 1, lines 11-14).

Therefore, in contrary to the Applicant's statement, i.e., bus interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen, Barrenscheen is clearly suggesting the claimed subject matter "multiplexer (i.e., Bus Interface BI1 in Fig. 4)" receiving first data from a processor (e.g., Module BU11 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) and transfers the received first data to a first memory (e.g., Module BU12 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) through a synchronous data bus (i.e., BUS1 in Figs. 2A-B) synchronized with the processor (See Barrenscheen, paragraph [0035], lines 11-12; for example, DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A),

or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor (See Barrenscheen, paragraph [0035], lines 11-12; for example, DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A). In other words, the recited claiming language "multiplexer," and its function in the exemplary claim 1 are interpreted as the bus interface BI1 performs the functions of and is described as the claimed subject matter "multiplexer" in Barrenscheen.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Further, the Examiner maintains that BUS1 in Figs. 2A-B is synchronized with the processor. Barrenscheen, however, does not indicate in paragraph [0035], lines 11-12 or Figs. 2A-B that BUS1 or BUS2 is synchronized with the processor. Although the DTU used as a DMA in paragraph [0035] can transfer data between BUS1 and BUS2, and between their respective devices, Barrenscheen does not require BUS1 or BUS2 to be synchronized with the processor in Figs. 2A-B or paragraph [0035]. Barrenscheen is silent with respect to this feature. ..." in the Response page 10, lines 1-9, the Examiner respectfully disagrees.

Basically, one of the ordinary skill in the art of digital computer system could understand that the statement "the DTU used as a DMA" in Barrenscheen, paragraph [0035], clearly anticipates the claimed limitation "a synchronous data bus synchronized with the processor," such that BUS1 (i.e., synchronous data bus) is synchronized with Module BU11 (i.e., processor) because it was well known in the art of digital computer system as a common knowledge at the time the invention was made.

Moreover, the Examiner doubts how the DTU can transmit data from one of the devices (i.e., Module BU11) to another device (i.e., Module BU12), which are connected to the BUS1, when

the DTU is used as a DMA controller if the BUS1 is not synchronized with the Module BU11, for example.

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Applicant submits that Masayuki (the primary reference) fails to teach or suggest both a synchronous data bus synchronized with a processor and an asynchronous data bus not synchronized with the processor, which is required in claims 2, 4, and 10. ... Moreover, Masayuki does not disclose any terms related to 'synchronous' and 'asynchronous'. Further, Applicant submits that it is not inherent that image data bus 33 is (asynchronous) not synchronized with CPU 41 in Fig. 2, because evidence of inherency in a reference 'must make it clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.' Continental Can Co. USA Inc. v. Monsanto Co., 948 F.2d 1264, 1269 (Fed. Cir. 1991) (emphasis added). ... Similarly, even if the image data bus 33 could either be synchronized or not synchronized with CPU 41, this possibility cannot be said to disclose that the image data bus is necessarily not synchronized when Masayuki is silent with respect to this feature. ... " in the Response page 11, line 1 through page 12, line 11, the Examiner respectfully disagrees.

Masayuki discloses a signal processing unit (See Title), wherein a synchronous data bus (i.e., CPU bus 34 of Fig. 2) synchronized with a processor (i.e., CPU 41 of Fig. 2) and an asynchronous data bus (i.e., image data bus 33 of Fig. 2) not synchronized with the processor (i.e., said image data bus being synchronized by sync generator 26 of Fig. 1, and said CPU being communicated via several interfaces in Fig. 1).

Even though the Applicant argues that Masayuki does not disclose any terms related to 'synchronous' and 'asynchronous', Masayuki discloses CPU (i.e., processor) and CPU bus (i.e.,

synchronized bus with said CPU), and further, image data bus (i.e., asynchronous data bus) being synchronized by Sync Generator in the Signal Processor, not being synchronized with said CPU (i.e., processor).

In contrary to the mere allegation of the Applicant's, i.e., it is not inherent that image data bus 33 is (asynchronous) not synchronized with CPU 41 in Fig. 2, Masayuki inherently suggests that said image data bus is not synchronized with CPU, such that memory controller 22 arbitrates said image data bus, and performs data transfer to CPU bus 34 in Fig. 1 (See Masayuki, paragraph [0036]). If said image data bus is synchronized with CPU, it is not necessary for said memory controller to perform said data transfer since said CPU could perform said data transfer (See Masayuki's prior art in Fig. 16, and paragraphs [0003]-[0006]), and furthermore, host interface 31 and JPEG interface 30, and memory interface 27 are not necessary for coupling to said CPU 41 in Fig. 1. In other words, the Applicant's essential arguments, i.e., Masayuki does not disclosure any terms related to 'synchronous' and 'asynchronous', and the claimed limitation "image data bus is (asynchronous) not synchronized with CPU," is inherently disclosed because the arguing elements are necessarily present in Masayuki because of the objective of Masayuki invention, i.e., signal processing unit prevents delay of image data bus (See Masayuki, paragraphs [0007]-[0010]).

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on Tuesday through Friday at 9:00am - 3:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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